Glossary

A-B

32-Bit Program A program compiles to run in 32-bit mode. For example, programs compiled for the PA RISC 1.x processors.

64-Bit Program A program compiled to run in 64-bit mode. For example, programs compiled for the PA-RISC 2.0 processor in wide mode.

Adapter Card Physical hardware, under software control, which is typically attached either directly to an I/O bus or to an auxiliary bus (e.g. SCSI) attached to a directly connected adapter. A device typically combines a hardware controller with the mechanism (e.g. disk controller with disk).

100BT 100BASE-T is the technical term for the Fast Ethernet or IEEE802.3u standard.

ARP Address Resolution Protocol.

Attach Chain A linked list of driver attach routines (<drv>_attach). As a hardware module is being configured, this list is walked to allow each driver in the system a chance to recognize and claim the hardware module.

Auto load A capability made possible via the DLKM feature. It occurs when the kernel detects a particular loadable module is required to accomplish some task, but the module is not currently loaded. The kernel automatically loads the module. During an auto load, the kernel also loads any modules that the module being loaded depends upon, just as it does during a demand load.

BAR Base Address Register. On a PCI card, one of the registers in PCI configuration space that contains the size and alignment requirements needed to map the card's registers. Each one also contains information (encoded in the low-order bits of the register) indicating whether they are base registers for PCI memory space or for PCI I/O space. The system reads and decodes this information and writes a PCI address back into these registers when it initially maps them in. Base address registers contain PCI addresses when set up.

Beta Semaphore Mutually-exclusive, blocking semaphores. When a thread acquires a beta semaphore, it is released. The owning thread may subsequently block (i.e., sleep) and still keep ownership. Threads waiting to acquire an owned beta semaphore are blocked.

BN-CDIO Bus Nexus CDIO, software that manages platform-dependent bus connection hardware.

Bus Mastering The act of taking over a bus and generating cycles on it. A bus master is any piece of hardware that creates read or write cycles on the PCI bus. Typical cards become bus masters only when they perform DMA, although any card-initiated cycle (for example, a peer-to-peer transaction) is an example of bus mastering.

Bus Nexus Connection between two buses.

C

Cache Coherence Consistency of data in host memory as viewed by processor caches and I/O devices.

CDIO Context-Dependent I/O module. A module in GIO framework which contains all bus specific and/or driver environment specific functionality.
Central Bus CDIO (CB-CDIO)
The BN-CDIO which is responsible for discovering and initializing CEC components.

Class A logical grouping of device or hardware modules by type. For instance the ‘class tape’ would include all tape devices regardless of bus interface.

Coherent I/O Accesses to data in host memory by I/O devices are consistent with accesses by processor caches. Hardware in the platform maintains the consistent view of data in host memory as DMA transactions flow through the hardware.

Continuous DMA A type of DMA that makes a host memory buffer continuously available to an I/O device. This type of DMA is mainly used for control structures and circular queues that are shared between the device driver and the hardware device.

Core Electronics Complex (CEC) The chip set which interfaces directly to the processor in the processor-memory interconnect. In simple systems, this usually includes memory controllers and I/O Adapters. On more complex systems, it might include high-speed interconnects and coherency controllers.

DLKM Dynamically Loadable Kernel Module. A feature available in HP-UX 11.0 that supports dynamic loading and unloading of kernel modules, to avoid wasting kernel memory by keeping modules in core when they are not in use.

DLPI Data Link Provider Interface
routine is linked to a system vector table. When an interrupt occurs, it is routed to the ISR that is placed in the section of the Interrupt Vector Table that corresponds to the received interrupt.

**Instance** A number assigned to an I/O tree node. The number is unique within a driver class.

**I/O Adapter** Hardware to provide IOVA translation between an I/O bus and the processor/memory interconnect. Devices on the I/O bus issue bus transactions to IOVA memory targets and the I/O adapter translates IOVA memory targets to physical addresses. The I/O adapter also participates in the coherency protocol of the processor caches for platforms that are coherent or semicoherent.

**I/O Bus** Interconnect bus for I/O cards and devices. PCI is an example of an I/O bus.

**I/O Node** An element of an I/O tree which includes all relevant information needed for configuring a single hardware module.

**I/O PDIR** I/O Page Directory. Address translation table associated with an I/O adapter. The I/O PDIR is analogous to the PDIR used by processors for virtual-to-physical address translations. It is a table maintained by the kernel to provide mappings between IOVAs and physical addresses.

**I/O Tree** Data structure for recording the I/O subsystem configuration information.

**IOVA** I/O Virtual Address. Address used by I/O devices to access host memory. Platforms that are semicoherent or coherent, or where the processor/memory interconnect is greater than 32 bits wide, generally implement IOVAs.

**IP** Internet Protocol.

**ISC** Interface Select Code. Usually used as a pointer to an element of a table of **isc_table_type** structures (one per interface card). Each ISC entry is used by WSIO to maintain interface device driver information.

**ISR** Interrupt Service Routine. A driver-specific routine which handles interrupts from the device.

**ISV** Independent Software Vendor

**J-M**

**Kernel module** A section of code responsible for supporting a specific capability or feature. Normally, such code is maintained in individual object files and/or archives, enabling modules to be conditionally included or excluded from the kernel, depending on whether or not the features they support are desired.

**LAN** Local Area Network.

**LP64** C language data model where the int data type is 32 bits wide, but long and pointer data types are 64 bits wide.

**LVM** The Logical Volume Manager is a disk management subsystem that offers access to filesystems as well as features such as disk mirroring, disk spanning, and dynamic partitioning.

**MAC** Medium Access Control.
Glossary

Map PCI Device/Function

**Map PCI Device/Function**
The act of mapping a PCI device or function involves determining the size and alignment requirements for each memory or I/O range described by an implemented configuration-space base register. Using these requirements, PCI Services finds a suitable hole in the memory or I/O address space and updates the corresponding base register to point to this range. This is taken care of by the system (firmware and/or the kernel) at the time of the card's initialization.

**Map PCI to Port Handle**  Mapping a PCI I/O space address to a port handle is the act which allows a driver to access the I/O space using `pci_read_port_uintNN_isc()` and `pci_write_port_uintNN_isc()`, passing in the port handle as a argument. The mapping is done through a call to `pci_get_port_handle_isc()`.

**Map PCI to Virtual Address**  Mapping a PCI memory space address to a virtual address is the act that allows a driver to access PCI space using `READ_REG_UINTNN_ISC()` or `WRITE_REG_UINTNN_ISC()` with that virtual address. The mapping is done through a call to `map_mem_to_host()`.

**Memory Mapped I/O (MMIO)** I/O that occurs by mapping the device’s I/O to system memory.

**MP** Multi-Processor

**MP Safe** Describes a module which is protected in an MP environment through the use of various spinlocks and semaphores. Note that MP-safeness does not imply any performance considerations due to the granularity of the semaphores (e.g., use of a single I/O Empire semaphore or separate semaphores for each instance all imply MP-safeness).

**MP Scalable** Describes an MP module which may add components without causing more drain on other MP modules. An MP-scalable driver will provide a separate spinlock for each instance of the driver. Non MP-scalable drivers may still be MP-safe but perhaps only provide a single semaphore and spinlock for all instances of the driver. Adding more instances of a non MP-scalable driver will therefore cause additional taxing of those resources for each instance added to the system.

**Module type** A module type is distinguished by the mechanism used to maintain the modules of that type within the kernel. DLKM modules are classified according to a fixed number of supported module types.

**Modwrapper** The additional code and data structures added to a DLKM module in order to make it dynamic.

**N-Q**

**NIC** Network Interface Card.

**Noncoherent I/O** Accesses to data in host memory by I/O devices are not made consistent with processor caches by hardware. Software must explicitly flush the processor caches prior to starting a DMA transaction by an I/O device; and, in the case of data read from an I/O device, purge the processor caches after the DMA transaction completes.
On-Line Addition and Replacement (OLA/R) The ability to insert adapter cards and replace such cards while a system is being used (Hot Plug).

PA Precision Architecture. When referring to buses, these are buses which conform to the Precision I/O Architecture.

Packet DMA A type of DMA that maps a host memory buffer temporarily. This is used when pre-existing memory objects must be mapped for DMA, or when a mapping only needs to be temporary.

PCI Peripheral Component Interconnect. An industry standard bus used mainly by current generations of HP platforms as a means of providing expansion I/O.

PCI Address An address in the PCI memory or I/O space. This is the type of address found in a PCI memory or I/O base address register. It is NOT a virtual address or an I/O port handle, which a driver could use to access a card.

PCI Card A PCI bus can have up to 32 devices; each device can have up to eight functions. A PCI card can have single or multiple devices; each device can have single or multiple functions. For example, a four-port LAN card is a multi-device PCI card, but none of these devices is multi-functional. On the other hand, a dual-port SCSI card is a single device, but it has two functions.

PCI Configuration Space This always-accessible space allows a driver to configure and obtain status from PCI devices or functions.

PCI I/O Space The ‘space’ that is addressed by an I/O cycle on the PCI bus. This is a less often used way to access card registers on cards who choose to respond to PCI I/O accesses. Most cards have registers that are in PCI memory space instead of I/O space (i.e., they respond to PCI memory cycles, not PCI I/O cycles). PCI memory space The space that is addressed by a memory cycle on the PCI bus. It is called memory space to indicate that it is memory-mapped input/output, as opposed to a special I/O style of input/output. Typical cards map their registers into PCI memory space, meaning they can only be accessed by PCI memory cycles.

PCI Memory Space The “space” that is addressed by a memory cycle on the PCI bus. It is called memory space to indicate that it is memory-mapped input/output, as opposed to a special “I/O” style of input/output. The current PA Workstation I/O architecture allows the PA processor to directly access PCI memory space (i.e., a single instruction). Typical cards map their registers into PCI memory space, meaning they can only be accessed by PCI memory cycles.

Physical Address Real address by which host memory or an I/O device register is accessed.

Port Handle The kernel resource associated with a mapped range of PCI I/O space. This handle is used to access the I/O space addresses by calling pci_read_port_uintNN_isc() and pci_write_port_uintNN_isc().

Port I/O (PIO) Communication with an I/O device using the device’s ports.

PPA Physical Point of Attachment
Glossary

SAP

R-S

SAP Service Attach Point

SCSI Small Computer System Interface. An industry standard external I/O bus available on all HP9000 systems.

Semicohrent I/O Similar to coherent I/O. However, for the case of data read from an I/O device, software must synchronize the data that have been read into host memory after the DMA transaction completes.

Series700 HP9000/7XX family of PA-RISC workstations.

Series800 HP9000/8XX family of PA-RISC business servers.

SIO Server I/O; I/O environment for port-server drivers with origins in S/800 systems.

SNAP Sub-Network Access Point

Spinlock Basic locking primitive used by the kernel for short-term locks. When a thread acquires a spinlock, the thread’s current processor becomes the effective owner until the spinlock is released. Threads (processors) waiting to acquire an owned spinlock will spin while waiting; they do not block. For the duration that a processor owns a spinlock, external interrupts to the processor are disabled.

Stream A connection supported by the STREAMS facilities between a user process and a device driver. It is a structure made up of linked modules, each of which processes the transmitted information and passes it to the next module. You can use STREAMS to connect to a wide variety of hardware and software configurations, using building blocks, or modules, that can be stacked together. STREAMS drivers and modules are similar in that they both must declare the same structures and provide the same interface. Only STREAMS drivers manage physical hardware and must therefore be responsible for handling interrupts if appropriate.

T-Z

Virtual Address Address used by processors, when executing in virtual mode, to access host memory. Address translation hardware converts a virtual address to a physical address before host memory is accessed. Virtual addresses may also be used to map and access I/O device registers.

WSIO Workstation and Server I/O; I/O environment for reentrant drivers with origins in S/700 systems and converged with S/800 systems.