Glossary

A

32-Bit Program A program compiled to run in 32-bit mode. For example, programs compiled for the PA RISC 1.X processors.

64-Bit Program A program compiled to run in 64-bit mode. For example, programs compiled for the PA-RISC 2.0 processor in wide mode.

100BT 100BASE-T is the technical term for the Fast Ethernet or IEEE802.3u standard. See also, Fast Ethernet.

Adapter Card Physical hardware, under software control, which is typically attached either directly to an I/O bus or to an auxiliary bus (e.g., SCSI) attached to a directly connected adapter. A device typically combines a hardware controller with the mechanism (e.g., disk controller with disk).

Area Allocator The memory attribute based allocated in HP-UX kernel which replace the old MALLOC()/FREE() interface. The advanced features include object caching, improved fault isolation, reduced memory fragmentation and better scaling.

ARP Address Resolution Protocol.

Attach Chain A linked list of driver attach routines (<drv>_attach). As a hardware module is being configured, this list is walked to allow each driver in the system a chance to recognize and claim the hardware module.

B

BAR Base Address Register. On a PCI card, one of the registers in PCI configuration space that contains the size and alignment requirements needed to map the card's registers. Each BAR also contains information (encoded in the low-order bits of the register) indicating whether they are base registers for PCI memory space or for PCI I/O space. The system reads and decodes this information and writes a PCI address back into these registers when it initially maps them in. BARs contain PCI addresses when properly set up.

BDR Boot Data Record.

Beta Semaphores Mutually-exclusive, blocking semaphores. When a thread acquires a beta semaphore, it is released. The owning thread may subsequently block (i.e., sleep) and still keep ownership. Threads waiting to acquire an owned beta semaphore are blocked.

Big Endian A format for storage or transmission of binary data in which the most significant bit or byte comes first. See also, Little Endian.

bit mask A pattern of binary values, typically used in bitwise operations.

Bit An atomic unit of data representing either a 0 or a 1.

Bitwise Operation A bitwise operation treats its operands as a vector of bits rather than a single number.

BN-CDIO Bus Nexus CDIO, low-level kernel software that manages platform-dependent bus connection hardware.

Broadcast Address A well-known multicast address signifying the set of all stations.

Bundle A collection of filesets, possibly from several different products, “encapsulated” for a specific purpose. Bundles can consist of groups of filesets or products.

Bus Mastering The act of taking over a bus and generating cycles on it. A bus master is any piece of hardware that creates read or write cycles on the PCI bus. Typical cards become bus masters only when they perform DMA operations, although any card-initiated cycle (for example, a peer-to-peer transaction) is an example of bus mastering.

Bus Nexus Connection between two buses.

C

Cache Coherence Consistency of data in host memory as viewed by processor caches and I/O devices.

Cacheline The smallest unit of memory that can be transferred between the main memory and the cache. Typically, Cacheline is hardware dependent.
Canonical format Synonymous with Little Endian format.

ccNUMA Cache-Coherent Non-Uniform Memory Architecture. See also, NUMA.

CDB Command Descriptor Block.

CDIO Context Dependent I/O module. A module in GIO framework which contains all bus specific and/or driver environment specific functionality.

Central Bus CDIO (CB-CDIO) The BN-CDIO which is responsible for discovering and initializing CEC components.

CKO Checksum Offload.

Class A logical grouping of device or hardware modules by type. For instance the class “tape” would include all tape devices regardless of bus interface.

Coherent I/O Accesses to data in host memory by I/O devices are consistent with accesses by CPU caches. Hardware in the platform maintains the consistent view of data in host memory as DMA transactions flow through the hardware.

Continuous DMA A type of DMA that makes a host memory buffer continuously available to an I/O device. This type of DMA is mainly used for control structures and circular queues that are shared between the device driver and the hardware device.

Core Electronics Complex (CEC) The chipset which interfaces directly to the processor in the processor-memory interconnect. In simple systems, this usually includes memory controllers and I/O adapters. On more complex systems, it might include high-speed interconnects and coherency controllers.

CPU Central Processing Unit

CSMA/CD Carrier Sense, Multiple Access with Collision Detection.

Datagrams (1) A frame or packet transferred using connectionless communications. (2) A frame or packet sent using best-effort service. (3) An IP packet.

Decapsulation The process of removing protocol headers and trailers to extract higher-layer protocol information carried in the data payload. See also, Encapsulation.

Depot A repository of software products managed by SD/UX. A depot consists of a directory or physical media such as tapes, CD-ROMS, or DVDs.

Device Driver The software used to provide an abstraction of the hardware details of a network or peripheral device interface. Device drivers allow higher-layer entities to use the capabilities of a device without having to know or deal with the specific implementation of the underlying hardware.

DLKM Dynamically Loadable Kernel Module.

DLPI Data Link Provider Interface.

DLSAP Data Link Service Access Point.

DMA Direct Memory Access. I/O transactions for which the device interacts directly with memory without processor intervention.

Driver Software module which controls a device, interface card or bus-nexus. See also, Device Driver

DSAP Destination Service Access Point.

Encapsulation The process of taking data provided by a higher-layer entity as the payload for a lower-layer entity and applying a header an trailer as appropriate for the protocol in question. See also, Decapsulation.

ENET HP-UX sample Native STREAMS DLPI network interface driver.

Ethernet The popular name for a family of LAN technologies standardized by IEEE 802.3.
**Fast Ethernet** An Ethernet system operating at 100 Mb/s.

**Filesets** Include all the files and scripts that make up a product. They can only be part of a single product. They are the lowest level object managed by SD.

**Fragmentation** A technique whereby a packet is subdivided into small packets so that they can be sent through a network with a smaller MTU. See also, Reassembly.

**Frame** The Data Link layer encapsulation of transmitted or received information

**Frame Check Sequence** A block check code used to detect errors in a frame. Most LANs use a CRC-32 polynomial as their FCS.

**Full Duplex** A mode of communication whereby a device can simultaneously transmit and receive data across a communications channel. See also, Half-duplex.

**G**

**Gigabit Ethernet** An Ethernet system operating at 1000 Mb/s.

**GIO** General I/O System.

**Group Address** Synonymous with multicast address.

**High Availability (HA)** Used to describe a computer system that has been designed to allow users to continue with specific applications even though there has been a hardware or software failure.

**HP-DLPI’s** HP’s own implementation of the DLPI layer.

**H**

**Half duplex** A mode of communication in which a device can either transmit or receive data across a communications channel, but not both simultaneously. See also, Full duplex.

**HBA** Host Bus Adapter.

**Header** A protocol-specific field or fields that preceed the encapsulated higher-layer data payload (e.g., the MAC addresses in a Data Link frame). See also, Trailer.

**Init Function** This is an attribute in driver modules modmeta file. An “initfunc” statement specified an initialization function, provided y the module, that the system should call during driver initialization.

**Init List** A linked list of device driver init routines (<drv>_init) which is built as the drivers configure themselves and run as the I/O system configuration is completed to perform any device driver-specific initialization.

**Installed Product Database (IPD)** SD uses the Installed Product Database (IPD) to keep track of what software is installed on a system. The IPD is a series of files and subdirectories that contain information about all the products that are installed under the root directory (/). For depots, this information is maintained in catalog files beneath the depot directory. The SD commands automatically add to, change and delete IPD and catalog information as the commands are executed.

**Interface Select Code (ISC)** Each instance of an adapter card has an ISC entry that the system maintains in an internal table. Each ISC entry is used by WSIO to maintain interface device driver information.

**Interface Service Routine (ISR)** A function that handles interrupts that are received for a specific device driver. A pointer to this routine is linked to a system vector table. When an interrupt occurs, it is
routed to the ISR that is placed in the section of the Interrupt Vector Table that corresponds to the received interrupt.

**Interrupt Service Routine** A function that handles interrupts that are received for a specific device driver. A pointer to this routine is linked to a system vector table. When an interrupt occurs, it is routed to the ISR that is placed in the section of the Interrupt Vector Table that corresponds to the received interrupt.

**Instance** A number assigned to an I/O tree node. The number is unique within a driver class.

**I/O Adapter** Hardware to provide IOVA translation between an I/O bus and the processor/memory interconnect devices on the I/O bus issue bus transactions to IOVA memory targets and the I/O adapter translates IOVA memory targets to physical addresses. The I/O adapter also participates in the coherency protocol of the processor caches for platforms that are coherent or semicoherent.

**I/O Bus** Interconnect bus for I/O cards and devices. PCI is an example of an I/O bus.

**I/O Node** An element of an I/O tree which includes all relevant information needed for configuring a single hardware module.

**I/O PDIR** I/O Page Directory. Address translation table associated with an I/O adapter. The I/O PDIR is analogous to the PDIR used by CPUs for virtual-to-physical address translations. It is a table maintained by the kernel to provide mappings between IOVAs and physical addresses.

**I/O Tree** Data structure for recording the I/O subsystem configuration information.

**IOVA** I/O Virtual Address. Address used by I/O devices to access host memory. Platforms that are semicoherent or coherent, or where the processor/memory interconnect is greater than 32-bits wide, generally implement IOVAs.

**IPF** Itanium Processor Family.

**IRQ** Interrupt Request.

**ISC** Interface Select Code. Usually used as a pointer to an element of a table of *isc_table_type* structures (one per interface card). Each ISC entry is used by WSIO to maintain interface device driver information.

**ISCSI** SCSI over IP.

**ISR** Interrupt Service Routine. A driver-specific routine which handles interrupts from the device.

**ISV** Independent Software Vendor

**J**

**Jumbo Frame** A frame longer than the maximum frame length allowed by a standard. Specifically used to describe the 9-Kbyte frames on Ethernet LANs.

**K**

**Kcweb** The HP-UX Kernel Configuration tool user interface uses as a web browser.

**L**

**LAN** Local Area Network. A network with a relatively small geographical extent.

**LBI** Line Based Interrupt.

**Length Encapsulation** The Ethernet frame format where the length/Type field contains the length of the encapsulated data rather than a protocol type identifier. Length Encapsulated frames typically use LLC to multiplex among multiple higher-layer protocol clients. See also, Type Encapsulation.

**Little Endian** A format for storage or transmission of binary data in which the least significant bit or byte comes first. See also, Big Endian.

**LLC** Line Based Interrupt.

**Logical Address** See Multicast Address.

**LP64** C language data model where the *int* data type is 32 bits wide, but long and pointer data types are 64 bits wide.

**LSB** Least significant bit or least significant bit.
LUN Logical Unit Number.

LVM The Logical Volume Manager is a disk management subsystem that offers access to file systems as well as features such as disk mirroring, disk spanning, and dynamic partitioning.

M

MAC Medium Access Control.

MAC Address A bit string that uniquely identifies one or more devices or interfaces as the sources or destination of transmitted frames. IEEE 802 MAC addresses are 48 bits in length and may be either unicast (source or destination) or multicast (destination only).

MAC Algorithm The set of procedures used by the stations ion a LAN to arbitrate for access to the shared communication channel (e.g., CSMA/CD, Token Passing).

Map PCI Device/Function The act of mapping a PCI device or function involves determining the size and alignment requirements for each memory or I/O range described by an implemented configuration-space base register. Using these requirements, PCI Services finds a suitable hole in the memory or I/O address space and updates the corresponding base register to point to this range. This is taken care of by the system (firmware and/or the kernel) at the time of the card's initialization.

Map PCI to Port Handle Mapping a PCI I/O space address to a port handle is the act which allows a driver to access the I/O space using pci_read_port_uintNN_isc() and pci_write_port_uintNN_isc(), passing in the port handle as a argument. The mapping is done through a call to pci_get_port_handle_isc().

Map PCI to Virtual Address Mapping a PCI memory space address to a virtual address is the act that allows a driver to access PCI space using READ_REG_UINTNN_ISC() or WRITE_REG_UINTNN_ISC() with that virtual address. The mapping is done through a call to map_mem_to_host().

mbuf Message buffer. Data structure used in mass storage stack.

Metadata The metadata for a module are used by the kernel configuration tools when configuring a module, they are also used by various kernel services while the module is in use.

Memory Mapped I/O (MMIO) I/O that occurs by mapping the device's I/O to system memory.

MP Multi-Processor

MP Safe Describes a module which is protected in an MP environment through the use of various spinlocks and semaphores. Note that MP-safeness does not imply any performance considerations due to the granularity of the semaphores (e.g., use of a single I/O Empire semaphore or separate semaphores for each instance all imply MP-safeness).

MP Scalable Describes an MP module which may add components without causing more drain on other MP modules. An MP-scalable driver will provide a separate spinlock for each instance of the driver. Non MP-scalable drivers may still be MP-safe but perhaps only provide a single semaphore and spinlock for all instances of the driver. Adding more instances of a non MP-scalable driver will therefore cause additional taxing of those resources for each instance added to the system.

Modwrapper The additional code and data structures added to a DLKM module to make it dynamic.

MSB Most significant bit, or most significant byte.

MTU Maximum Transmission Unit.

MTU Discovery A process whereby a station can determine the largest frame or packet that can be transferred across a internetwork without requiring fragmentation.

Multicast Address A method of identifying a set of one or more stations as the destination for transmitted data. Also known as logical address or group address.

N

NFS Network File System.
NIC Network Interface Card or Network Interface Controller.

Noncoherent I/O Accesses to data in host memory by I/O devices are not made consistent with processor caches by hardware. Software must explicitly flush the processor caches prior to starting a DMA transaction by an I/O device; and, in the case of data read from an I/O device, purge the processor caches after the DMA transaction completes.

NUMA Non-Uniform Memory Architecture. A memory architecture, used in multiprocessors, where the access time depends on the memory location. A processor can access its own local memory faster than non-local memory (memory which is local to another processor or shared between processors). See also, ccNUMA.

O

On-Line Addition, Replacement and Delete (OLA/R/D) The ability to insert adapter cards and replace such cards while a system is in use (Hot Plug).

Operating System The low-level software responsible for managing the underlying hardware in a computer, scheduling tasks, allocating storage.

OSI Open Systems Interconnect.

P

PA Precision Architecture.

Package A collection of files that need to be distributed. It is created by a SD command.

Packet The Network layer encapsulation of transmitted or received information.

Packet DMA A type of DMA that maps a host memory buffer temporarily. This is used when pre-existing memory objects must be mapped for DMA, or when a mapping only needs to be temporary.

PCI Peripheral Component Interconnect. An industry standard bus used mainly by current generations of HP platforms as a means of providing expansion I/O.

PCI Address An address in the PCI memory or I/O space. This is the type of address found in a PCI memory or I/O base address register. It is NOT a virtual address or an I/O port handle, which a driver could use to access a card.

PCI Card A PCI bus can have up to 32 devices; each device can have up to eight functions. A PCI card can have single or multiple devices; each device can have single or multiple functions. For example, a four-port LAN card is a multi-device PCI card, but none of these devices is multi-functional. On the other hand, a dual-port SCSI card is a single device, but it has two functions.

PCI Configuration Space This always-accessible space allows a driver to configure and obtain status from PCI devices or functions.

PCI I/O Space The space that is addressed by an I/O cycle on the PCI bus. This is a less often used way to access card registers on cards which choose to respond to PCI I/O accesses. Most cards have registers that are in PCI memory space instead of I/O space (i.e., they respond to PCI memory cycles, not PCI I/O cycles).

PCI Memory Space The space that is addressed by a memory cycle on the PCI bus. It is called memory space to indicate that it is memory-mapped input/output, as opposed to a special I/O style of input/output. The current PA Workstation I/O architecture allows the PA processor to directly access PCI memory space (i.e., a single instruction). Typical cards map their registers into PCI memory space, meaning they can only be accessed by PCI memory cycles.

Physical Address Real address by which host memory or an I/O device register is accessed.

Physical Layer The lowest layer of the seven-layer OSI model, responsible for transmission and reception of signals across the communication medium.

Ping A utility program used to test for network connectivity by using the Echo Request and Echo Response mechanisms of ICMP.
**Port Handle** The kernel resource associated with a mapped range of PCI I/O space. This handle is used to access the I/O space addresses by calling `pci_read_port_uintNN_isc()` and `pci_write_port_uintNN_isc()`.

**Port I/O (PIO)** Communication with an I/O device using the device’s ports.

**PPA** Physical Point of Attachment

**Product** Collections of filesets and (optionally) subproducts and control scripts.

**Product Specification File (PSF)** A master file where all bundle configuration information (attributes) exists.

**Promiscuous Mode** A mode of operation of a network interface in which it receives (or attempts to receive) all traffic regardless of Destination Address.

**Protocol** A set of behavioral algorithms, message formats, and message semantics used to support communications between entities across a network.

**pSCSI** Parallel SCSI. See also, SCSI.

**Q**

**QLISP** HP-UX sample parallel

**R**

**Reassembly** The process of reconstructing a packet from its fragments. See also, Fragmentation.

**Root** In SD, a system on which depot software is installed.

**S**

**SAM** System Administration Manager. A GUI based application for HP-UX system administration.

**SAP** Service Attach Point

**SCSI** Small Computer System Interface. An industry standard external I/O bus available on all HP9000 systems.

**SDTR** Synchronous Data Transfer Request.

**Semicoherent I/O** Similar to coherent I/O. However, for the case of data read from an I/O device, software must synchronize the data that have been read into host memory after the DMA transaction completes.

**Server I/O (SIO)** I/O environment for port-server drivers with origins in S/800 systems.

**SNAP** Sub-Network Access Point

**Software Distributor (SD)** The software distributor tool for HP-UX operation system.

**Software Objects** Can be a bundle, product or filesets.

**Spinlock** Basic locking primitive used by the kernel for short-term locks. When a thread acquires a spinlock, the thread’s current processor becomes the effective owner until the spinlock is released. Threads (processors) waiting to acquire an owned spinlock will spin while waiting; they do not block. For the duration that a processor owns a spinlock, external interrupts to the processor are disabled.

**Stream** A connection supported by the STREAMS facilities between a user process and a device driver. It is a structure made up of linked modules, each of which processes the transmitted information and passes it to the next module. Use STREAMS to connect to a wide variety of hardware and software configurations, using building blocks, or modules, that can be stacked together. STREAMS drivers and modules are similar in that they both must declare the same structures and provide the same interface. Only STREAMS drivers manage physical hardware and must therefore be responsible for handling interrupts if appropriate.

**T**

**Target** Either a host (the host’s file system) or a depot that resides on a host.

**TBI** Transaction Based Interrupt.

**TCP** Transmission Control Protocol.

**Token Ring** A LAN whose MAC algorithm uses token passing among stations on a logical ring topology (i.e., IEEE 802.5).
**Topology** The physical or logical layout of a network.

**Trailer** A protocol-specific field or fields that follow the encapsulated higher-layer data payload (e.g., the FCS in a Data Link Frame). See also, Header.

**Type Encapsulation** The Ethernet frame format in which the Length/Type field identifies the protocol type of the encapsulated data rather than its length. See also, Length Encapsulation.

**U**

**UDP** User Datagram Protocol.

**V**

**Virtual Address** Address used by processors, when executing in virtual mode, to access host memory. Address translation hardware converts a virtual address to a physical address before host memory is accessed. Virtual addresses may also be used to map and access I/O device registers.

**W**

**WDTR** Wide Data Transfer Request.

**WSIO** Workstation and Server I/O. A CDIO, also the HP-UX Driver Development Environment (DDE).