Absolute Address
See Physical Address.

Access Rights
A function of virtual address translation that controls access to each page through privilege levels for read, write, execute, and gateway. The TLB contains, within each entry, information used to determine who may have access to that page. This information is divided into two groups: (1) page access (access ID) which is used to determine if a process or user may access a page; and (2) the access rights field that is combined with the user’s privilege level and the WD bit of the PID register to determine if the type of access the user is requesting will be allowed.

Address
PA-RISC is a byte-addressable system which uses both virtual and absolute addresses. A virtual address can be split into two parts: the high-order bits which are the space identifier and the low-order bits that give the offset within the space. Absolute addresses do not have space identifiers; only a 64-bit offset. Doublewords, words, and halfwords are always located at addresses which are aligned to their size (in bytes). Quadwords are aligned on doubleword boundaries.

Address Translation
For a virtual memory system, the process whereby the virtual (logical) address of data or instructions is translated to its absolute address in physical memory.

Aliasing
The condition when the same physical memory location is accessed by different virtual addresses or by both an absolute and a virtual address.

Alter
The action of setting the E-bit of a TLB entry to 0 and modifying some portion of the physical page number field. Altered entries in the TLB are still visible to software through the insert TLB protection instructions.

Architecture
Refers to the time-independent functional appearance of a computer system. An implementation of an architecture is an ensemble of hardware, firmware, and software that provides all the functions as defined in the architecture.

Arithmetic and Logical Unit (ALU)
The part of a PA-RISC processor that performs arithmetic and logic operations on its inputs, producing output and status information.
Assist Processor
A processor which may be added to the basic PA-RISC system to enhance performance or functionality for algorithms which experience substantial gains from the use of specialized hardware. Assist processors are differentiated by the level at which they interface with the memory hierarchy. (See special function units and coprocessors).

B-bit (Taken Branch in Previous Cycle)
A bit in the PSW that is 1 if the previous instruction was a taken branch.

Base Register
A register that holds the numeric value that is used as a base value in the calculation of addresses. Displacements or index values are added to this base value.

Base-Relative Branch
When a general register is used as the base offset to obtain the target address, the branch is called base relative.

Biased Exponent
The exponent field for a floating-point number. It consists of the true exponent plus the bias.

Binary Floating-point Number
A number format consisting of the three components: sign, exponent, and significand.

Block TLB
A block TLB provides fixed address translations which map address ranges larger than a page.

Byte
A group of eight contiguous bits which is the smallest addressable unit on a PA-RISC system.

C-bit (Code Address Translation Enable)
A bit in the PSW that specifies whether virtual address translation of the instruction address is to be performed.

Cache
A high-speed buffer unit between main memory and the CPU. The cache is continually updated to contain recently accessed contents of main memory to reduce access time. When a program makes a memory request, the CPU first checks to see if the data is in the cache so that it can be retrieved without accessing memory. There may be one cache for both instructions and data or separate caches for each.
Cache Coherence
The property of multiple caches whereby they provide identical shared memory images. Processors in a multiprocessor system are said to be cache coherent if they provide the image of single cache.

Cache Control Hint
A 2-bit field in some memory reference instructions which provides a hint to the processor on how to resolve cache coherence. The processor may disregard the hint without compromising system integrity, but performance may be enhanced by following the hint.

Cache Miss
A cache miss occurs when the cache does not contain a copy of the cache line being requested by the address. The cache is updated with data and re-accessed.

Carry/Borrow Bits
A 16-bit field in the PSW that indicates if a carry or borrow occurred from the corresponding nibble (4 bits) as a result of the previous arithmetic operation.

Central Processing Unit (CPU)
The part of a PA-RISC processor that fetches and executes instructions.

Check
The interruption condition when the processor detects an internal or external malfunction. Checks may be either synchronous or asynchronous with respect to the instruction stream.

Coherence Check
An action taken by hardware to insure coherence.

Combined TLB
Some systems have a TLB which provides address translation for both instruction and data references.

Compatibility
The ability for software developed for one machine type to execute on another machine type. PA-RISC provides compatible execution of application programs written for earlier-generation Hewlett-Packard computer systems.

Completer
A machine instruction field used to specify instruction options. Typical options include address modification, address indexing, precision of operands, and conditions to be tested to determine whether to nullify the following instruction.
Condition
The state of a value or a relationship between values used in determining whether an instruction is to branch, nullify, or trap.

Control Register (CR)
A register which contains system state information used for memory access protection, interruption control, and processor state control. A PA-RISC processor contains 25 control registers (7 more are reserved).

Coprocessor
A type of assist processor which interfaces to the memory hierarchy at the level of the cache. Coprocessors are special purpose units that work with the main processor to speed up specialized operations such as floating-point arithmetic and graphics processing. Coprocessors generally have their own internal state and hardware evaluation mechanism.

Coprocessor Configuration Register (CCR)
The CCR (in CR 10) is an 8-bit register which records the presence and usability of coprocessors. Each bit position (0-7) corresponds to the coprocessor with the same unit number. Setting a bit in the CCR to 1 enables the use of the corresponding coprocessor, if present and operational. If a CCR bit is 0, the corresponding coprocessor, if present, is logically decoupled and an attempt to reference the coprocessor causes an assist emulation trap.

Current Instruction
The instruction whose address is in the front element of the instruction address queues (IASQ and IAOQ).

D-bit (Data Address Translation Enable)
A bit in the PSW that specifies whether virtual address translation of data addresses is to be performed.

Data Cache (D-cache)
A high-speed storage device which contains data items that have been recently accessed from main memory. The D-cache can be accessed independently of the instruction cache (I-cache) and no synchronization is performed.

Data TLB (DTLB)
A separate TLB which does address translation only for data memory references.

Denormalized Numbers
Any non-zero floating-point number with the exponent field all zeros. Denormalized numbers are distinguished from normal numbers in that the value of the “hidden” bit to the left of the implied binary point is zero.
Dirty
A block of memory (commonly a cache line or a page) which has been written to is referred to as dirty.

Disabling an Interrupt
A disabled interrupt is prevented from occurring. The interruption does not wait until re-enabled and it is not kept pending.

Displacement
The amount that is added to a base register to form an offset in the virtual address computation.

Dynamic Displacement
If the displacement value is computed during the course of program execution and is obtained from a general register, it is called dynamic.

E-bit (Little Endian Memory Access Enable)
A bit in the PSW which determines whether memory references assume big endian or little endian byte ordering.

Effective Address
The address of the operand for the current instruction, derived by applying specific address building rules.

Equivalently Aliased
A condition when two virtual addresses map to the same physical address, and where the two addresses are identical in the following bits: Offset bits 12 through 31. If the use of space bits in generating the cache index is enabled, the addresses must also be identical in these bits: Space Identifier bits 36 through 39, 44 through 47, and 52 through 63.

Equivalently Mapped
A condition when a virtual address is equal to its absolute address.

Exponent
The part of a binary floating-point number that normally signifies the integer power to which two is raised in determining the value of the represented number.

External Branch Instructions
The target of these instructions may lie in a different address space than that of the instruction. The external branch instructions are: BE and BLE.
External Interrupt Enable Mask (EIEM)

The EIEM (CR 15) is a 64-bit register containing one bit for each external interrupt class. When set to 0, bits in the EIEM mask interruptions pending for the external interrupts corresponding to those bit positions.

External Interrupt Request Register (EIR)

The EIR register (CR 23) is a 64-bit register containing one bit for each external interrupt. When set to 1, a bit designates that an interruption is pending for the corresponding external interrupt.

F-bit (Performance Monitor Interruption Unmask)

A bit in the PSW used to unmask the performance monitor interruption.

Fault

The interruption condition when the current instruction requests a legitimate action which cannot be carried out due to a system problem such as the absence of a main memory page. After the system problem is cleared, the faulting instruction will execute normally. Faults are synchronous with respect to the instruction stream.

Floating-point Register (FPR)

A storage unit which constitutes the basic resource of the floating-point coprocessor. Floating-point registers are at the highest level of memory hierarchy and are used to load data from and store data to memory and hold operands and results of the floating-point coprocessor. The floating-point coprocessor contains 32 double-precision (64-bit) floating-point registers which may also be accessed as 64 single-precision (32-bit), or 16 quad-precision (128-bit) registers.

Following Instruction

The instruction whose address is in the back element of the instruction address queues (IASQ and IAOQ). This instruction will be executed after the current instruction. This instruction is not necessarily the next instruction in the linear code space.

Fraction

The portion of the significand explicitly contained in a binary floating-point number. The rest of the significand is the “hidden” bit to the left of the implied binary point. The “hidden” bit normally has the value one.

G-bit (Debug Trap Enable)

A bit in the PSW used to enable data and instruction debug traps.

General Register (GR)

A storage unit which constitutes the basic resource of the CPU. General registers are at the highest level of memory hierarchy and are used to load data from and store data to memory and hold operands and results from the ALU. A PA-RISC processor contains 32 general registers.
H-bit (Higher Privilege Transfer Trap Enable)
   A bit in the PSW that enables an interruption whenever the following instruction will execute at a higher privilege level.

High-Priority Machine Check (HPMC)
   An interruption which occurs when a hardware error has been detected which requires immediate attention.

I-bit (External, Power Failure, and LPMC Interruption Unmask)
   A bit in the PSW used to unmask external interrupts, power failure interrupts, and low-priority machine check interruptions.

IAOQ (Instruction Address Offset Queue)
   A two-element queue of 64-bit registers that is used to hold the Instruction Address offset (IA offset). The first element is IAOQ_Front and holds the IA offset of the current instruction. The other element is IAOQ_Back and holds the IA offset of the following instruction.

IA-Relative Branches
   When a displacement is added to the current Instruction Address offset (IA offset) to obtain the target address, the branch is called IA relative.

IASQ (Instruction Address Space Queue)
   A two-element queue of up to 64-bit registers that is used to hold the Instruction Address space (IA space). The first element is IASQ_Front and holds the IA space of the current instruction. The other element is IASQ_Back and holds the IA space of the following instruction.

IIAOQ (Interruption Instruction Address Offset Queue)
   A two-element queue of 64-bit registers that is used to save the Instruction Address offset for use in processing interruptions.

IIASQ (Interruption Instruction Address Space Queue)
   A two-element queue of up to 64-bit registers that is used to save the Instruction Address space for use in processing interruptions.

Infinity
   The binary floating-point numbers that have all ones in the exponent and all zeros in the fraction. The values of these two numbers are distinguished only by the sign. Thus, they are +∞ and −∞.

Instruction Cache (I-cache)
   A high-speed storage device that contains instructions that have been recently accessed from main memory. The I-cache can be accessed independently of the data cache (D-cache) and no synchronization is performed.
Instruction TLB (ITLB)
A separate TLB which does address translation only for instructions.

Interrupt
The interruption condition when an external entity (such as an I/O device or the power supply) requires attention. Interrupts are asynchronous with respect to the instruction stream.

Interruption
An event that changes the instruction stream to handle exceptional conditions including traps, checks, faults, and interrupts.

Interrupt Instruction Register (IIR)
The IIR (CR 19) is used by the hardware to store the instruction that caused the interruption or the instruction that was in progress at the time the interruption occurred.

Interrupt Offset Register (IOR)
The IOR (CR 21) receives a copy of the offset portion of a virtual address at the time of an interruption whenever the PSW Q-bit is 1. The value copied is dependent upon the type of interruption.

Interrupt Parameter Registers (IPRs)
The Interruption Instruction Register or IIR (CR 19), Interruption Space Register or ISR (CR 20), and Interruption Offset Register or IOR (CR 21) are collectively termed the Interruption Parameter Registers or IPRs. They are used to pass the interrupted instruction and a virtual address to an interruption handler. These registers are set (or frozen) at the time of an interruption when the PSW Q-bit is 1. The IPRs can be read reliably only when the PSW Q-bit is 0. The values saved in these registers are dependent upon the type of interruption.

Interrupt Processor Status Word (IPSW)
The IPSW (CR 22) receives the value of the PSW when an interruption occurs. The layout of IPSW is identical to that of PSW and it always reflects the machine state at the point of interruption.

Interrupt Space Register (ISR)
The ISR (CR 20) receives a copy of the space portion of a virtual address at the time of an interruption whenever the PSW Q-bit is 1. The value copied is dependent upon the type of interruption.

Interrupt Vector Address (IVA)
The IVA (CR 14) contains the absolute address of an array of service procedures assigned to interruptions.
Interspace Branches

When the target of the branch lies in a different address space as that of the branch instruction, it is referred to as an interspace branch.

Intraspace Branches

When the target of the branch lies in the same address space as that of the branch instruction, it is referred to as an intraspace branch.

Interval Timer

Two internal registers which are both accessed through Control Register 16. The Interval Timer is a free-running counter that signals an interruption when equal to a comparison value.

Invalidate

The action of setting the E-bit of a TLB entry to a 0, leaving the virtual page number and physical page number fields unchanged. Invalid entries in the TLB are still visible to software through insert TLB protection instructions.

L-bit (Lower Privilege Transfer Trap Enable)

A bit in the PSW that enables an interruption whenever the following instruction will execute at a lower privilege level.

Local Branch Instructions

The target of these instructions always lie in the same address space as that of the instruction.

Low-Priority Machine Check (LPMC)

An interruption which occurs when a recoverable hardware error has been detected.

M-bit (High-Priority Machine Check Mask)

A bit in the PSW that disables the recognition of an HPMC.

Many-Reader/One-Writer Non-Equivalent Aliasing

A condition where multiple virtual addresses are non-equivalent aliases. Generally, before enabling a write-capable translation, any non-equivalent read-only aliases must be disabled, and the affected address range flushed from the cache. Similarly, before re-enabling the read translation(s), the write-capable translation must be disabled, and the affected address range flushed from the cache.

Masking an Interrupt

A masked interrupt can still be recognized as a pending event but occurrence of the interrupt is delayed until it is unmasked.
Memory

A device capable of storing information in binary form. The term “memory” typically refers to main memory.

Memory Address Space

The memory address space consists of absolute addresses in the range 0x0000000000000000 through 0xEFFFFFFFFFFFFFFF.

Memory-mapped I/O

Control of input and output through load and store instructions to particular virtual or physical addresses.

Move-in

The action of bringing data or instructions into a cache.

Multiprocessor

A computer with multiple processors.

NaN

The binary floating-point numbers that have all ones in the exponent and a non-zero fraction. NaN is the term used for a binary floating-point number that has no value (i.e., “Not a Number”). The two types of NaNs, quiet and signaling, are distinguished by the value of the most significant bit in the fraction field. A zero indicates a quiet NaN and a one indicates a signaling NaN.

Non-Equivalently Aliased

A condition when two virtual addresses map to the same physical address, but do not meet the requirements for equivalently aliased addresses. (See “Equivalently Aliased” on page A-5.)

Nullify

To nullify an instruction is equivalent to skipping over that instruction. A nullified instruction has no effect on the machine state (except that the IA queues advance and the PSW B, N, X, Y, and Z bits are set to 0). The current instruction is nullified when the PSW N-bit is 1.

P-bit (Protection Identifier Validation Enable)

A bit in the PSW that is used as a protection identifier validation enable bit. If the P-bit is 1, the Protection Identifiers in control registers 8, 9, 12, and 13 are used to enforce protection.

Page

Virtual memory is partitioned into pages which can be resident in matching size blocks (called page frames) in memory. The smallest page size is 4096 bytes (4 Kbytes).

Page Group

Eight contiguous pages, with the first of these pages beginning on a 32-Kbyte boundary.
Physical Address

The address that is the result of the virtual address translation or any address that is not translated. A physical address is the concatenation of the physical page number and the offset. Physical addresses are also referred to as absolute addresses.

Privilege Level

The PA-RISC access control mechanisms are based on 4 privilege levels numbered from 0 to 3, with 0 being the most privileged. The current privilege level is maintained in the front element of the Instruction Address Offset Queue (IAOQ_Front).

Processor Status Word (PSW)

A 64-bit register which contains information about the processor state.

Q-bit (Interruption State Collection Enable)

A bit in the PSW that, when set to 1, enables collection of the machine state at the instant of interruption (IIASQ, IIAOQ, IIR, ISR, and IOR).

R-bit (Recovery Counter Enable)

A bit in the PSW that enables recovery counter trapping and decrementing of the Recovery Counter.

Read-Only Non-Equivalent Aliasing

A condition where multiple virtual addresses map to the same physical address, and where each virtual address has a read-only translation.

Recovery Counter

The Recovery Counter (CR 0) counts down by 1 during execution of each non-nullified instruction for which the PSW R-bit is 1.

Remove

The action of taking a TLB entry out of the TLB. Insertion of translations into the TLB, for example, causes other entries to be removed.

S-bit (Secure Interval Timer)

A bit in the PSW that, when set to 1, allows the Interval Timer to be read only by code executing at the most privileged level.

SFU Configuration Register (SCR)

The SCR (in CR 10) is an 8-bit register which records the presence and usability of SFUs (Special Function Units). Each bit position (0-7) corresponds to the SFU with the same unit number. Setting a bit in the SCR to 1 enables the use of the corresponding SFU if present and operational. If a SCR bit is 0, the corresponding SFU if present, is logically decoupled and an attempt to reference the SFU causes an assist emulation trap.
Shadow Register (SHR)

A register into which the contents of a general register are copied upon interruptions. A PA-RISC processor contains 7 shadow registers which receive the contents of GRs 1, 8, 9, 16, 17, 24, and 25. The contents of the shadow registers are copied back to these GRs by the RETURN FROM INTERRUPTION AND RESTORE instruction.

Shift Amount Register (SAR)

The SAR (CR 11) is used by the variable shift, extract, deposit, and branch on bit instructions. It specifies the number of bits or the ending bit position of a quantity that is to be shifted, extracted or deposited.

Sign

A one bit field in which one indicates a negative value and zero indicates a positive value.

Significand

The component of a binary floating-point number that consists of the implicit (or “hidden”) leading bit to the left of the implied binary point together with the fraction field to its right.

Space Identifier (Space ID)

An up to 64-bit value which combines with the offset to form the upper portion of a virtual address.

Space Register (SR)

A register used to specify the space identifier for virtual addressing. A PA-RISC processor contains 8 space registers.

Special Function Unit (SFU)

A type of assist processor which interfaces to the memory hierarchy at the general register level. It acts as an alternate ALU for the main processor and may have its own internal state.

Static Displacement

If the displacement is a fixed value that is known at compile time, it is called static.

Strong Ordering

The property that accesses to storage, such as loads and stores, appear to software to be done in program order. In multiprocessing systems, strong ordering means that accesses by a given processor appear to that processor as well as to all other processors in the system, to be done in program order.

System Mask

The W, E, O, G, F, R, Q, P, D, and I bits of the PSW are known as the system mask. Each of these bits, with the exception of the Q-bit, may be set to 1, set to 0, written, and read by the system control instructions that manipulate the system mask.
T-bit (Taken Branch Trap Enable)
A bit in the PSW that enables the taken branch trap.

Taken Branch
Conditional branches are considered to be “taken” if the specified condition is met. Unconditional branches are always “taken”.

TLB Entry
A virtual to physical address translation, either valid or invalid, which is present in the TLB. Entries are visible to software through either references (such as loads, stores, and semaphores) or insert TLB protection instructions (ITLBP and IDTLBP).

TLB Miss Handling
The action taken, either by hardware or software, on a TLB miss. This involves inserting the missing translation into the proper TLB.

TLB Miss
The condition when there is no entry in the TLB matching the current virtual page number. In this case, the TLB is updated either by software or by hardware.

TLB Slot
A hardware resource in the TLB which holds a TLB entry.

Translation Lookaside Buffer (TLB)
A hardware unit which serves as a cache for virtual-to-absolute memory address mapping. When a memory reference is made to a given virtual address, the virtual page number is passed to the TLB and the TLB is searched for an entry matching the virtual page number. If the entry exists, the absolute page number (contained in the entry) is concatenated with the page offset from the original virtual address to form an absolute address.

Trap
The interruption condition when either (1) the function requested by the current instruction cannot or should not be carried out, or (2) system intervention is requested by the user before or after the instruction is executed.

Virtual Addressing
A capability that eliminates the need to assign programs to fixed locations in main memory. Addresses supplied by a program are treated as logical addresses which are translated to absolute addresses when physical memory is addressed.

Write Disable (WD) Bit
The low-order bit of each of the four protection identifiers (PIPs) which, when 1, disables the use of that PID for validating write accesses.
X-bit (Data Memory Break Disable)

A bit in the PSW that disables the data memory break trap if equal to 1. A data memory break trap happens if a write is attempted to a page whose TLB B-bit is 1.

Y-bit (Data Debug Trap Disable)

A bit in the PSW that disables the data debug trap if equal to 1. A data debug trap happens if a memory reference is performed to an address which matches an enabled data breakpoint.

Z-bit (Instruction Debug Trap Disable)

A bit in the PSW that disables the instruction debug trap if equal to 1. An instruction debug trap happens if an attempt is made to execute an instruction at an address which matches an enabled instruction breakpoint.