Overview

Procera Networks and Intel have joined forces to deliver a high performance Deep Packet Inspection (DPI) solution that significantly decreases the time to market for networking equipment manufacturers to add industry leading Layer 7 application classification and metadata extraction capabilities to their solutions.

The combination of Procera’s Network Application Visibility Library (NAVL) and Intel’s Data Plane Development Kit (DPDK) addresses the pressing need for telecommunications and enterprise equipment providers to implement application-aware policies that enable them to efficiently manage their networks while ensuring high Quality of Experience (QoE) for all network users. This solution can be deployed in a variety of networking scenarios including Network Security (IDS/IPS, DPI, DLP), Cyber Security, Network Monitoring, Data Forensics, Network Probes, Policy Enforcement, Analytics and Big Data processing.

Why This Solution?

The explosive growth in the types of security and networking solutions requiring DPI is pushing the industry to deliver high performance solutions with extensive metadata extraction while maintaining zero packet loss. The combination of Procera’s NAVL DPI engine with Intel’s DPDK provides the performance and footprint required to meet the high performance demands of today’s telecom and enterprise equipment manufacturers.

Performance and Footprint

A well-known problem with legacy DPI solutions is the negative impact on processor performance and memory, latency, jitter and packet loss. This is where the Procera/Intel solution rises above all others. The Procera/Intel solution is made to inspect packets at high wire speeds with minimal effects on latency, jitter and packet loss while maintaining industry leading performance for application classification and metadata extraction. It is critical to keep the amount of resources required low for integrated DPI and application classification technology. The fewer cores (on a multi-core processor) and the less on-board memory an engine needs, the better. Maintaining a small footprint with high performance helps contain costs for network infrastructure vendors and their customers.
Layer 7 Application Classification and Metadata Extraction

Procera Networks’ Network Application Visibility Library (NAVL) features next generation DPI technology, providing real-time, Layer-7 application classification and metadata extraction for network traffic. NAVL uses a combination of deep packet inspection and application classification techniques to deliver industry leading coverage and accuracy of network traffic. In addition, the sophisticated hierarchical data flow architecture produces the fastest throughput performance and lowest memory footprint in the market. NAVL is delivered as an OEM Software Development Kit (SDK) to dramatically reduce the time, cost and complexity of adding DPI technology and application intelligence to your enterprise or telecom solutions.

- **Classification Techniques** – NAVL uses multiple classification techniques, including deep protocol dissection, surgical pattern matching, heuristic analysis, flow association and more to ensure that applications are accurately classified.

- **Metadata Extraction** – NAVL provides an extensive list of metadata elements including details related to content type, user information, application performance, video quality, etc.

- **Customizable Integration Options** – the NAVL team works closely with customers to ensure integration works seamlessly with vendor products. We provide tools to assist with integration including sample code, metadata and trace files.

- **Application Coverage** – NAVL classifies today’s most popular and relevant applications including mobile, social networking, P2P, instant messaging, file sharing, enterprise and Web 2.0. For a complete list of application coverage, please visit www.applabs.proceranetworks.com.

Packet Processing on Intel Architecture

With Intel® processors, it’s possible to transition from using discrete architectures per major workload (application, control, packet, and signal processing) to a single architecture that consolidates the workloads into a more scalable and simplified solution. As a result, developers may be able to eliminate special-purpose hardware such as network processors (NPUs), co-processors, application specific integrated circuits (ASICs), and field-programmable gate arrays (FPGAs).

This is possible, in large part, due to the Intel® Data Plane Development Kit (Intel® DPDK), a set of software libraries that can improve packet processing performance by up to ten times. As a result, it’s possible to achieve over 80 Mpps throughput on a single Intel® Xeon® processor and double that with a dual-processor configuration.

This solution is ideal for telecom wireless infrastructure evolved packet core (EPC) applications and other network elements. Packet processing while executing other workloads on an Intel processor reduces hardware costs, simplifies the application development environment, and reduces time to market. The Intel DPDK is also playing a critical role in software-defined networking (SDN) and network functions virtualization (NFV).

Another way to cut system costs is to do away with various add-on acceleration modules. Instead, use the acceleration modules that are already on Intel processor-based platforms with Intel® QuickAssist Technology and the Intel DPDK.